DETAILED ACTION

Specification

1. The abstract of the disclosure is objected to because it consists of more than 25 lines. Correction is required. See MPEP § 608.01(b).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

2. Claims 1, 2, 7, 9, 12, 13, 16, and 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sakamoto et al (US 2002/0001788).

Sakamoto teaches a thermal processing method comprising the steps of: holding a plurality of substrates in a wafer boat, conveying the wafer boat into the reaction chamber, heating a plurality of zones by means of a plurality of heating units, and forming thin films on a surface of the substrates by introducing a process gas into said reaction chamber. The thermal processing method further comprises: depositing a thin

film on a plurality of test wafers (1st substrates) located in each zone of the chamber, measuring the thickness of the deposited layer in each zone, setting the temperature in each zone based on the thickness of films deposited, depositing the thin film on a plurality of other test wafers (2nd substrates) using the set temperatures in the zones, measuring the thickness of the deposited films on the second set of test wafers, comparing the thickness with a predetermined thickness range, correcting the temperature of each zone based on the measured thickness of the deposited films, and depositing a thin film on a plurality of production substrates to form the finished products having a desired uniform film thickness (Fig. 1, [0056]-[0062], [0073]-[0078]).

Sakamoto does not explicitly disclose that thin films are deposited on the surface of the first test wafers by means of less consumption of the process gas than on the surfaces of the production substrates or that thin films are deposited on the surface of the second test wafers by means of more consumption of the process gas than on the surfaces of the first test wafers. However, since Sakamoto teaches an optimization of the temperature of the heaters to reach a desired thickness of deposited films, it would have been obvious to one of ordinary skill in the art to deposit a film below the desired target thickness on the first test wafers, adjust the temperature of the heaters accordingly, and deposit a thicker film on the second test wafers at the corrected temperature to reach the desired thickness of the film, wherein the deposition on the first test wafers would consume less process gas than the deposition of the second test wafers since the film deposited onto the first test wafers is thinner.

Regarding Claim 7, Sakamoto discloses that the heat treatment process may include thermal oxidation or CVD processes [0004].

Regarding Claim 9, Sakamoto teaches placing one test wafer in each zone (5 zones) of the chamber, however, since the wafer boat may hold for example 150 wafers, it would have been obvious to one of ordinary skill in the art to run a full batch (fully arranged in holding region) of test wafers if desired to more accurately achieve film uniformity throughout all portions of the wafer boat.

Regarding Claims 12, 13, 16, and 17, Sakamoto teaches an apparatus for carrying out the thermal processing method discussed above including a temperature setting part, a temperature correcting part, a temperature setting program, and a temperature correcting program (Fig. 1, [0066]-[0078]).

Thus, claims 1, 2, 7, 9, 12, 13, 16, and 17 would have been obvious within the meaning of 35 USC 103 over the teachings of Sakamoto.

3. Claims 3 and 4 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sakamoto as applied above in view of Yoo (US 2003/0162372).

Sakamoto teaches that an oxide film may be deposited by wet oxidation using H2 and O2 ([0144], [0148]), but does not teach activating the process gas to generate active species and forming oxide films by means of said active species.

Yoo teaches a method of forming an oxide film by wet oxidation using H2 and O2, wherein oxygen radicals are produced to enhance the oxidation rate (Abstract, [0008], [0041]).

It would have been obvious to one of ordinary skill in the art at the time of invention by applicant to generate active species such as the oxygen radicals suggested by Yoo in the wet oxidation process of Sakamoto in order to enhance the oxidation rate.

Thus, claims 3 and 4 would have been obvious within the meaning of 35 USC 103 over the combined teachings of Sakamoto and Yoo.

4. Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Sakamoto in view of Yoo as applied above and further in view of Applicant's Admitted Prior Art (Spec. p. 2, lines 19-26).

Sakamoto and Yoo do not teach that the first substrates are substrates on which oxide films having an average thickness of 50 nm or more have been formed in advance.

Applicant's Admitted Prior Art states that it was known in the art to use silicon oxide dummy wafers when adjusting the temperature set values of respective heaters to make the thickness of a deposited silicon oxide film uniform between wafers in a vertical furnace and cites JP-A-2001-77041 as an example of such an adjusting operation.

It would have been obvious to one of ordinary skill in the art at the time of invention by applicant to use a first substrate having an oxide film deposited thereon as suggested by Applicant's Admitted Prior Art as the first test wafers in the process of Sakamoto since silicon oxide dummy wafers were suitable for a temperature adjusting operation such as the adjusting operation of Sakamoto. Also, it would have been obvious to one of ordinary skill in the art to use a silicon oxide dummy wafer having an

oxide layer of any desired thickness, including values in the claimed range, especially absent evidence showing a criticality for using oxide thicknesses in the claimed range.

Thus, claim 5 would have been obvious within the meaning of 35 USC 103 over the combined teachings of Sakamoto, Yoo, and Applicant's Admitted Prior Art.

5. Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over Sakamoto in view of Yoo as applied above and further in view of Watanabe et al ('602).

Sakamoto and Yoo do not teach that the second substrates are bare silicon wafers.

Watanabe teaches that dummy wafers used in a vertical furnace reactor may be silicon wafers (Fig. 3, Col. 9, lines 37-50).

It would have been obvious to one of ordinary skill in the art at the time of invention by applicant to use silicon wafers as suggested by Watanabe as the test wafers (dummy wafers) in Sakamoto since silicon wafers would have been suitable as dummy wafers in vertical furnace reactors.

Thus, claim 6 would have been obvious within the meaning of 35 USC 103 over the combined teachings of Sakamoto, Yoo, and Watanabe.

6. Claims 10, 11, 14, and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sakamoto as applied above in view of Jun et al ('094).

Sakamoto does not teach arranging the production substrates at a portion on an upstream side of a flow of process gas in the holding region to be processed in the substrate holder and arranging the first substrates at a residual portion in the holding region.

Jun teaches a method of controlling the thickness of a deposited layer by loading monitoring wafers into a the substrate holder with production wafers, measuring the thickness of the film deposited on the monitoring wafers, and adjusting the temperature for each zone of the furnace in order to form a target thickness on the production substrates. Jun teaches that the monitoring wafers may be loaded into different zones of the furnace (which would include a residual portion) and production wafers are loaded with the monitoring wafers (including portions on an upstream side of a flow pf process gas) (Figs. 1, 4A, 4B, 5, Col. 2, lines 40-60, Col. 3, line 40-Col. 4, line 20).

It would have been obvious to one of ordinary skill in the art at the time of invention by applicant to arrange production wafers with the test wafers of Sakamoto, wherein the production wafers are arranged at a portion of the holding region on an upstream side of a flow of process gas and the test wafers are arranged in a residual region of the holding region as suggested by Jun in order to increase process productivity and reduce process cost (Jun, Col. 3, lines 50-55).

Regarding Claim 11, Sakamoto teaches that the flow rate of the process gas and time of thermal process are common in the corrected temperature step and the final step of forming a film on a production substrate since the only parameter that is changed is the temperature of the zones [0073]-[0078].

Regarding Claim 14, Jun discloses an apparatus for arranging the substrates as discussed above and it would have been obvious that Jun discloses a substrate conveying unit that conveys a substrate onto the substrate holder since monitoring

wafers are placed in specific portions of the wafer boat and production wafers fill the remaining portions.

Regarding Claim 15, Sakamoto teaches loading a specific number of substrates, such as 150 substrates [0058], onto a wafer boat and Jun teaches loading a specific number of monitoring wafers with production wafers onto a wafer boat, thus it would have been obvious to one of ordinary skill to use a part that judges the number of production substrates since the specific number of production substrates loaded in the wafer boat is known in both processes.

Allowable Subject Matter

7. Claim 8 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter: The prior art does not teach or suggest using first substrates having surfaces on which patterns have not been formed and second substrates having surfaces on which patterns have been formed in a temperature adjustment operation to control the thickness of a deposited film on a plurality of production substrates (third substrates).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to ELIZABETH A. BURKHART whose telephone number is (571)272-6647. The examiner can normally be reached on M-Th 7-5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy H. Meeks can be reached on 571-272-1423. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Elizabeth A Burkhart/
Examiner, Art Unit 1792

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